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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/610,497	06/30/2003	James Stuart Wight	CMA-0009	5376
21323	7590	06/30/2005		EXAMINER
TESTA, HURWITZ & THIBEAULT, LLP			TRINH, MICHAEL MANH	
HIGH STREET TOWER				
125 HIGH STREET			ART UNIT	PAPER NUMBER
BOSTON, MA 02110			2822	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/610,497	WIGHT ET AL.
Examiner	Art Unit	
Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 07 April 2005.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1 and 2 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1 and 2 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

*** This office action is in response to Applicant's amendment filed on April 07, 2005. Claims 1-2 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

1. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Busking et al (6,107,684) in view of Tamura et al (6,166,971) and Seshita (6,366,770).

Busking et al teach an integrated circuit package comprising an integrated circuit die 5 (Figs 2-4; col 2, line 53 through col 4) having at least one circuit etched thereon (col 1, lines 15-33), wherein the circuit comprises elements which require theoretical values, and wherein the circuit also includes a on-die component 8 of bond wires (Fig 3B; col 3, lines 20-35); and a housing 11 containing said integrated circuit die 5 (col 2, lines 53-67; col 3, lines 1-14), wherein the integrated circuit die 5 is electrically coupled to the housing using at least one wire bonds 4,6,8 (Figs 1A-4B); and wherein the at least wire bonds have an inductance associated therewith (col 3, lines 50-60; line 28 through col 4; Figs 5,1A-4B), wherein the theoretical values of the elements of the circuit required by the integrated circuit are actually incorporated into the circuit through the use of wire bonds having a pre-determined inductance values, and wherein the wire bond inductance is used to facilitate operation of the at least one circuit as the wire bonds are electrically coupled to the circuits formed in the die and generate an amount of inductance during operation. Busking also discloses a method comprising of making available wire bonds 4,6,8 for electrically connected to circuit formed in the die 5, wherein the wire bonds 4,6,8 generate an amount of inductance during operation of the circuits, so that inductance of the wire bonds are used to facilitate operation of a circuit contained in an integrated circuit package comprising making available wire bond inductance to the circuit from the wire bonds (Figs 5, 1A-4A, col 3, line 15 through col 4), wherein the circuit is contained in an integrated circuit die 5 housed in the integrated circuit package (Figs 1A-4B, col 2, line 53 through col 3).

Busking already teaches an integrated circuit die having at least one circuit including at least one elements 8, but lacks having the circuit comprising an impedance inverter (claim 2) having elements which require theoretically negative reactive component values (claim 1)

However, Gonda teaches (at col 3, lines 9-38) forming an integrated circuit die having at least one circuit, wherein the circuit comprising an impedance inverter (re claim 2, col 3, lines 9-20) which is having elements including negative inductance shunt arms, which elements require theoretically negative reactive component values (re claim 1). Seshita teaches (at Figs 1A,2; col 5, line 16 through col 6) forming an integrated circuit die having at least one circuit, wherein the circuit comprising inductor elements (MC1b, MC2b, MC3b) having theoretical values, wherein the theoretical values of the elements of the circuit required by the integrated circuit are actually incorporated into the circuit through the use of wire bonds 20h,20i,20j having a pre-determined inductance values, and wherein the wire bond inductance is used to facilitate operation of the at least one circuit.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit die having at least one circuit of Busking by forming at least one circuit comprising an impedance inverter, which is having elements which require theoretically negative reactive component values, as taught by Gonda and Seshita. This is because of the desirability to form an integrated circuit die of crystal oscillators that can be operated in the high frequency (HF) and ultra high frequency (UHF) band, and to serve as a buffer and impedance transformer between the low impedance output and the high impedance of a load, wherein using available wire bonds as an inductor element would save area for other devices, would reduce processing steps and production cost.

Response to Arguments

1. Applicant's remarks filed April 07, 2005 have been fully considered but they are not persuasive, and are also moot in view of the new ground(s) of rejection.

*** Forming the circuit comprising an impedance inverter which is having elements including negative inductance shunt arms, which elements require theoretically negative reactive component values is taught by Gonda (col 3, lines 9-20). As further taught by Seshita (at Figs 1A,2; col 5, line 16 through col 6), an integrated circuit die is formed to have at least one circuit, wherein the circuit comprising inductor elements (MC1b, MC2b, MC3b) having theoretical values, wherein the theoretical values of the elements of the circuit required by the integrated circuit are actually incorporated into the circuit through the use of wire bonds 20h,20i,20j having

a pre-determined inductance values, and wherein the wire bond inductance is used to facilitate operation of the at least one circuit.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oasc-3-16



Michael Trinh
Primary Examiner